

# White Paper: 40 Gb/s Backplane Ethernet Channel Characterization



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The design of 40 Gb/s (Gb/s = Gigabit per second) backplanes requires the selection of suitable connectors and PCB base materials. To ensure the performance of the backplane, it is crucial to define design rules based on channel simulations. At the same time, it is important to find the balance between costs and performance. Measurements validate whether the backplane is within the interconnect characteristics limits.

**Following comprehensive Signal Integrity (SI) simulations performed by HARTING and the PICMG (PCI Industrial Computer Manufacturers Group), HARTING was found to have the capabilities to design, simulate, manufacture and test 40 Gb/s backplanes.** This qualification process was initiated with the *PICMG 3.1 R2.0 “Ethernet/Fiber Channel for AdvancedTCA® Systems”* Specification. One of the main topics was the definition of the Backplane physical layer interface required to support 10GBASE-KR and 40GBASE-KR4 Ethernet characteristics. PICMG 3.0 is the AdvancedTCA® base specification, which includes board design guidelines targeting 3.125 Gb/s serial data rates. Signal Integrity simulations performed by HARTING and the PICMG sub-committee were part of the process, described below, to define the requirements and limits for the test fixtures and backplane assembly utilized by HARTING for such high speed backplanes.

## Interconnect characteristics

The interconnect parameters for the backplane Ethernet implementation were obtained from the IEEE802.3-2010. The Interconnect Characteristics in Annex 69B of this standard are informative limits, and the testing is based on S-Parameters. The analysis can be done based on measured or simulated S-Parameters or a mix of both.

### Interconnect parameters

- Fitted attenuation (FA)
- Insertion loss (IL)
- Insertion loss deviation (ILD)
- Insertion loss to crosstalk ratio (ICR)
- Return loss (RL)
- Crosstalk (XT)
- Power sum differential near-end crosstalk (PSNEXT)
- Power sum differential far-end crosstalk (PSFEXT)
- Power sum differential crosstalk (PEXT)

Backplane Ethernet is evolving, and the IEEE802.3bj standard to support 100Gbps (4 x 25.78125 Gb/s) is under development and is scheduled to be released in 2014.

## Backplane design flow

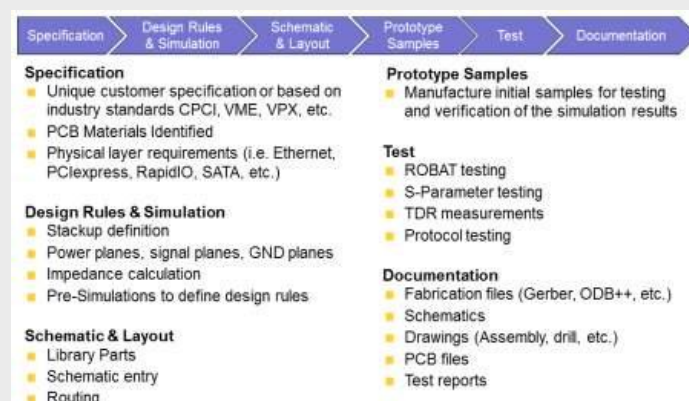


Figure 1: Backplane design flow

## Backplane design rules

Design rules include:

- Backplane material
- Backdrill/ max. stub length
- Routing guidelines
- Additional features

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The connector footprint has a strong impact on the results, and it is important to assign the layers (signal and ground power) properly and define the backdrill levels to reduce the stub length of the plated through-hole.

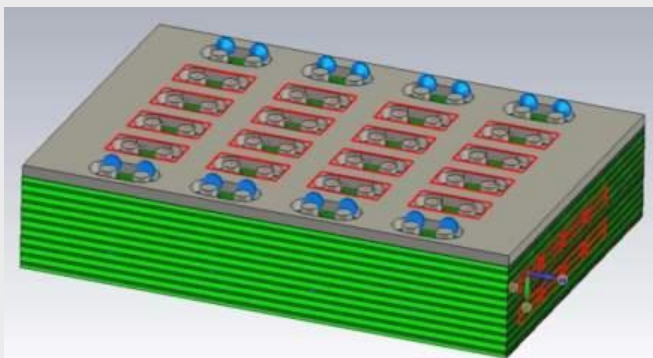


Figure 2: Connector footprint simulation

The stub length is the part of the plated through-hole underneath the traces for signal transmission. An example is shown in Figure 3.

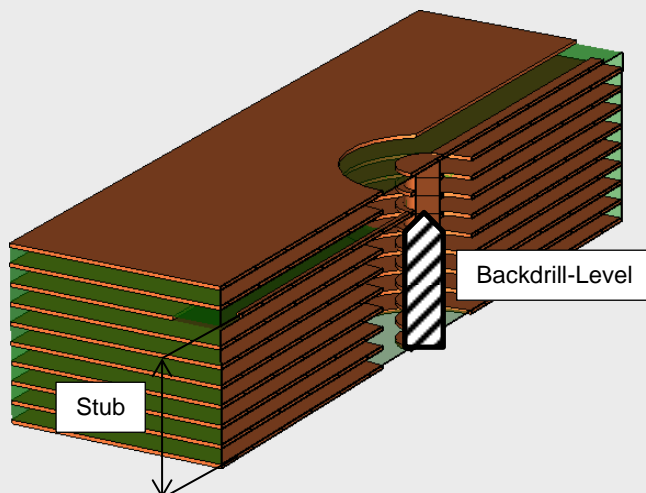


Figure 3: Example of a Plated Thru hole Stub

## Channel Simulation

Channel simulation analyzes the entire transmission path between defined test points and calculates interconnect parameters. The design rules are defined by simulation. The setup is complex and typically consists of many

sub circuits with S-Parameter files or other models. Each file has to be consistent and causal. It is recommended to program templates for the processing of the parameters to avoid time consuming, manual handling of the raw data and errors caused by this.

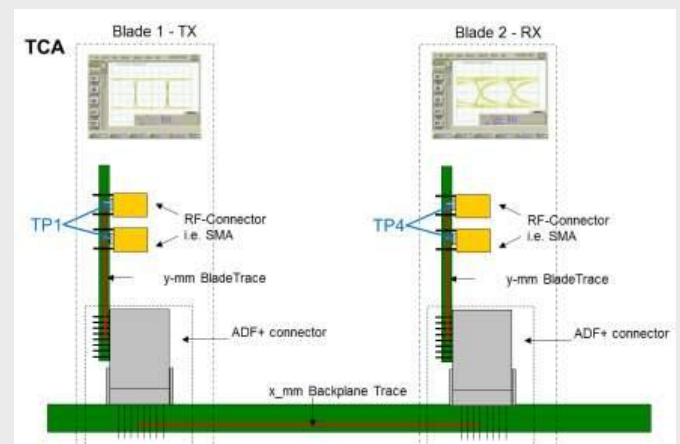


Figure 4: Channel reference points

Figure 4 shows the test points TP1 and TP4 for the AdvancedTCA® channel.

For backplane measurements and channel simulation the test fixtures need to meet the backplane test paddle card requirements

The simulation and data post processing is done in the Agilent Advanced Design System (ADS) software. HARTING developed comprehensive scripts and post processing to plot the required channel parameters in the desired format.

In the channel setup the models of the connector and footprints are included. For the channel simulation the corner parameters are analyzed to check the interconnect characteristics of two worse case channels with the longest stub length.

- Shortest Link
- Longest Link
- Worst case impedance

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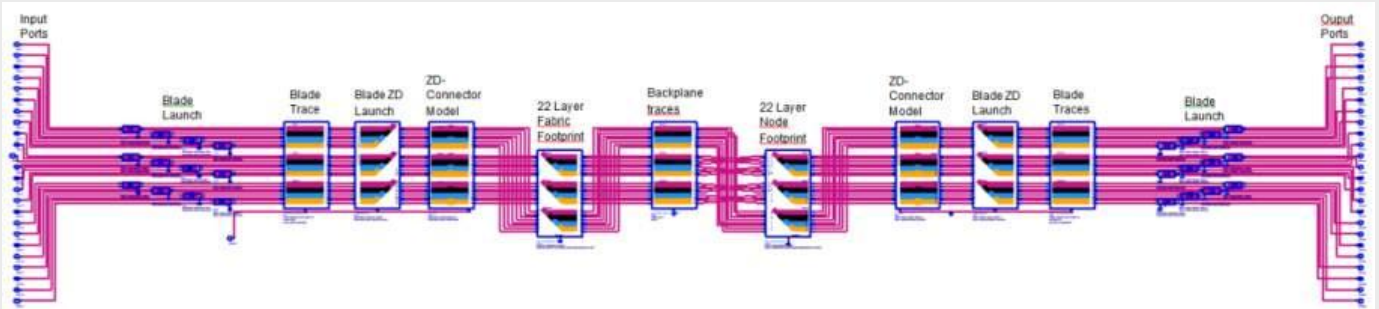


Figure 5: Simulation Channel Details

## Simulation Results

### Fitted attenuation (FA)

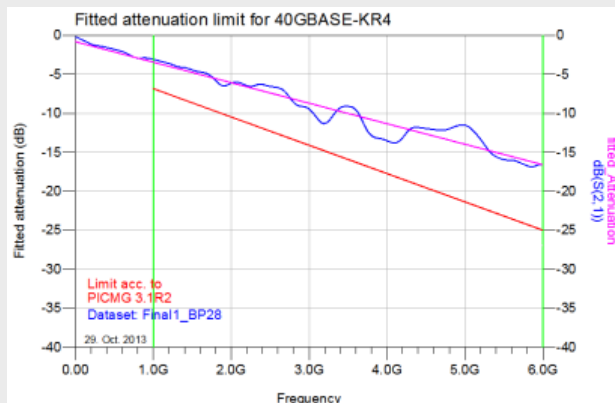


Figure 6: FA of the shortest worst case channel

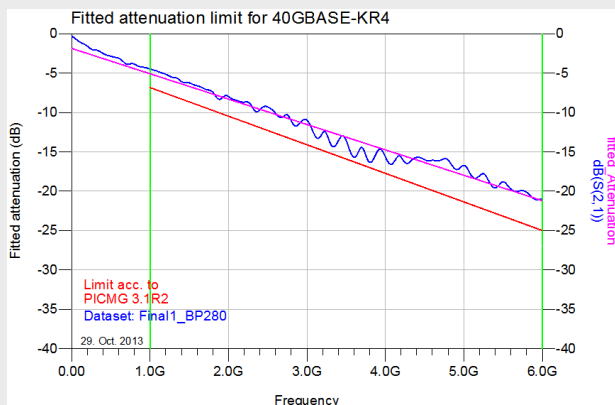


Figure 7: FA of the longest worst case channel

### Insertion Loss Deviation (ILD)

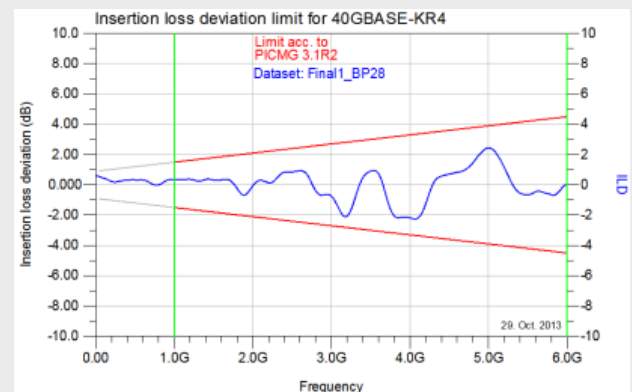


Figure 8: ILD of the shortest worst case channel

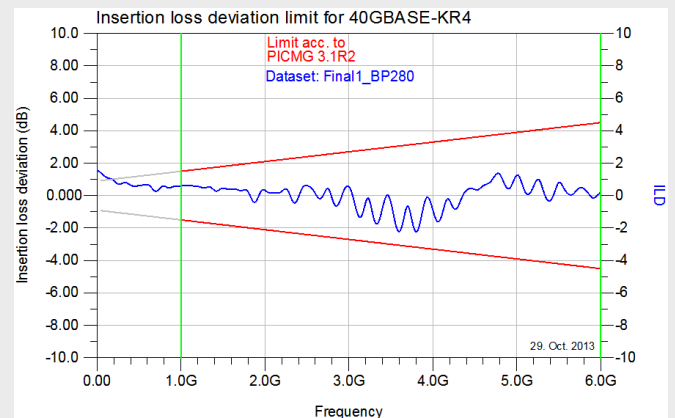


Figure 9: ILD of the longest worst case channel

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## Return loss (RL)

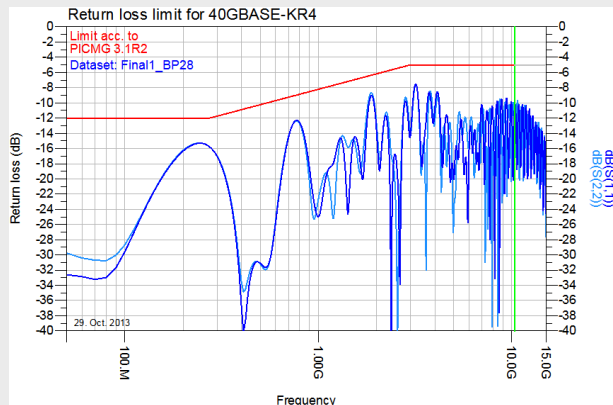


Figure 10: RL of the shortest worst case channel

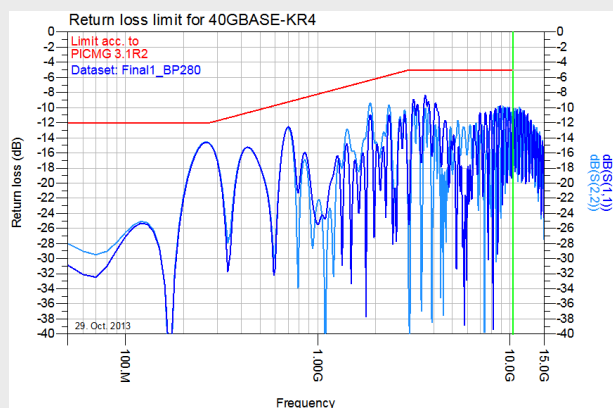


Figure 11: RL of the longest worst case channel

## Insertion loss to crosstalk ratio (ICR)

Insertion loss to crosstalk ratio (ICR) is the ratio of insertion loss to the total crosstalk (Power sum crosstalk). The fitted ICR is the least mean square log-linear fit to the ICR.

The victim pair is assigned to row CD of the ADFplus (ADF = Advanced Differential Fabric, plus= higher-fidelity version) connector and surrounded by 8 aggressor pairs.

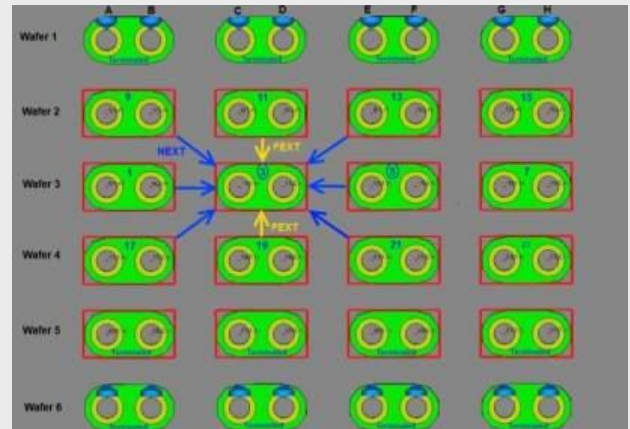


Figure 12: Assignment for Crosstalk simulation

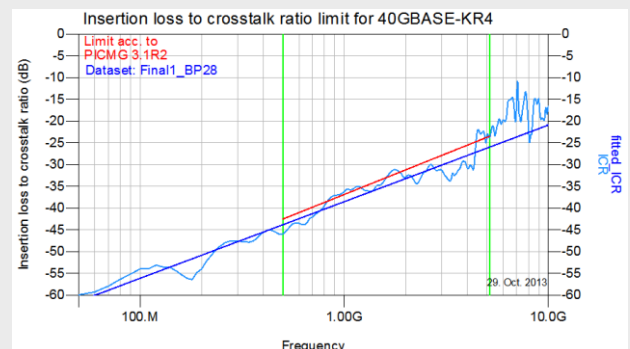


Figure 13: ICR of the shortest worst case channel

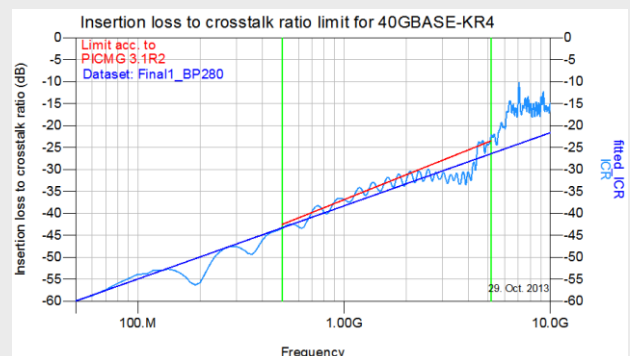


Figure 14: ICR of the longest worst case channel



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## Measurements

Backplane samples are first manufactured and then the verification of the simulations and design parameters are performed. These are both required to release the final backplane design and manufacturing data.

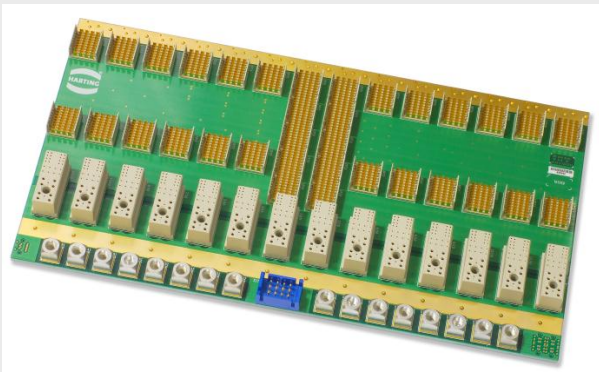


Figure 15: HARTING 40 Gb/s Backplane

The interconnect parameters of the backplanes are measured with a 4 Port Network Analyzer.



Figure 16: 4 Port Network Analyzer

Test fixtures are required for the backplane measurements. HARTING developed test fixtures with the ADFplus connector. The test cards have a strong impact on the results, and the connector launches are optimized with 3D field solvers.

Two test fixtures have been developed for ATCA backplane testing. The 10 layer Fixtures have 16 coaxial SMA connector launches allowing each signal contact to be tested or terminated with precision resistors.

The difference between both card types is the mounting layer of the SMA-connectors (One with SMAs on the top side and one with SMAs on the bottom side). This allows two adjacent or nearby configurations to be tested (the distance between the slots does not allow the use of right angled adapters).

The test cards provide short via stubs at the SMA connector due to back-drilling in four stages and reflect the typical design of line cards.



Figure 17: Test fixtures

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The trace length of approx. 68mm along with the low loss material is ideal to measure the backplane performance, but it does not reflect the high loss test fixtures required by PICMG 3.1 R2.0.

Chapter 5.4.6 defines the backplane channel performance including test fixtures compliant to Chapter 5.4.4 of PICMG 3.1 R2.

Chapter 5.4.6 ¶230:

*“Some test equipment may be capable of emulating the S-Parameter characteristics of part or all of the mated paddle card assembly. Alternatively the effects of test fixtures may be added to direct measurements through post-measurement computations. Either of these methods is allowed so long as the characteristics of the emulated/computed fixtures match the test fixture characteristics found within this specification.”*

For all compliance testing in this report the post measurement computation method is used to achieve the channel performance.

## Test fixture Compliance

- Fitted attenuation
- Insertion loss deviation
- Return loss
- Common mode return loss
- Common mode conversion loss
- Insertion loss to crosstalk ratio

## Test fixture measurement results

The following diagrams show the measurement results of the test fixture.

The test fixture including the ADFplus connector was characterized with a probe station.

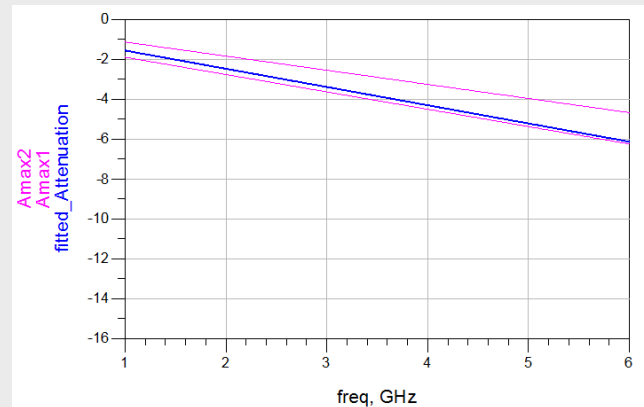


Figure 18: Test fixture Fitted attenuation

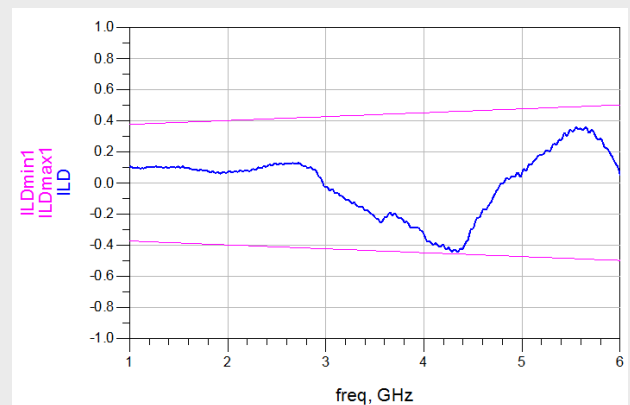


Figure 19: Test fixture Insertion loss deviation

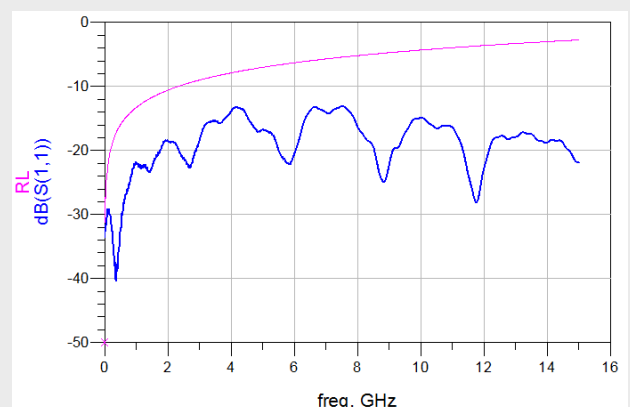


Figure 20: Test fixture Return loss

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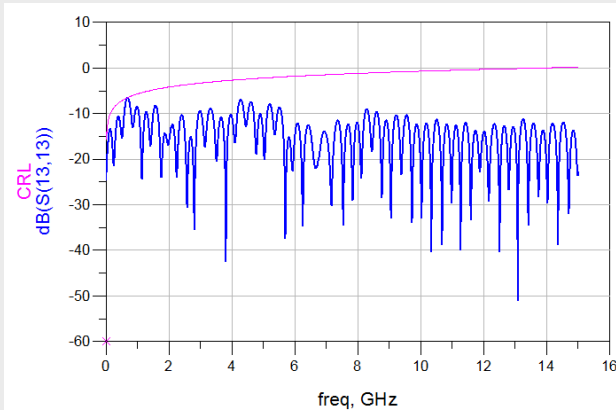


Figure 21: Test fixture Common mode return loss

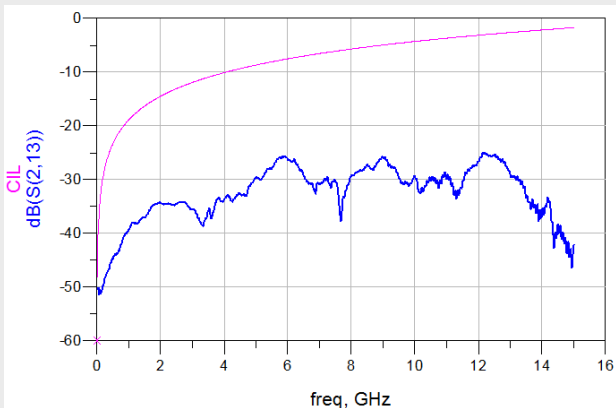


Figure 22: Test fixture Common Mode conversion loss

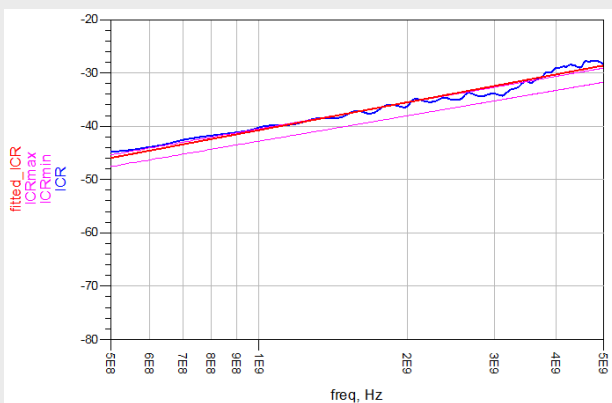


Figure 23: Test fixture Insertion loss to crosstalk ratio

The fitted ICR violates the maximum limit by less than one dB. This might be caused by the measurements with a probe station to derive the S-Parameters of the single test fixture as probes do not allow all adjacent contacts to be terminated. This adds some reflections on adjacent lines that result into additional crosstalk. Since this is a little bit more crosstalk than allowed, we see this as additional safety margin.

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## Measurement Results

### Fitted attenuation (FA)

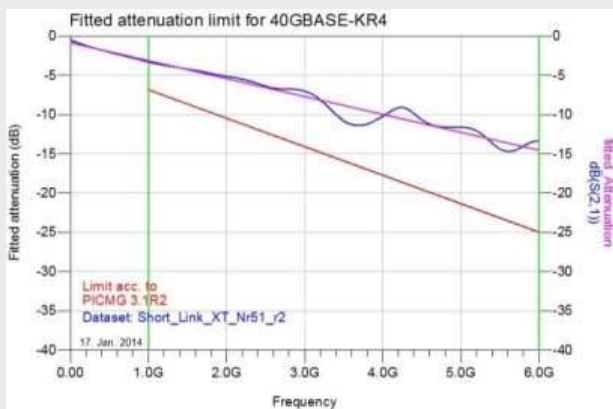


Figure 24: FA of the shortest worst case channel

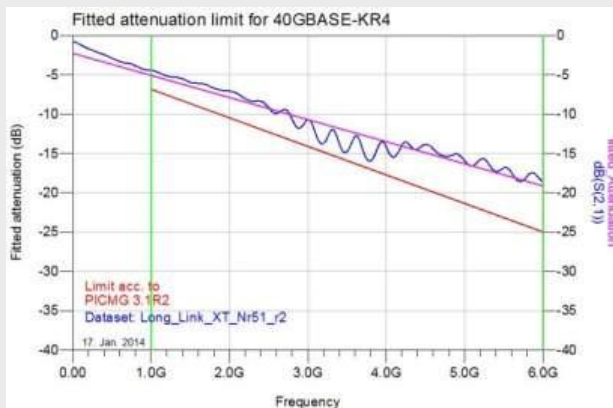


Figure 25: FA of the longest worst case channel

### Insertion loss deviation (ILD)

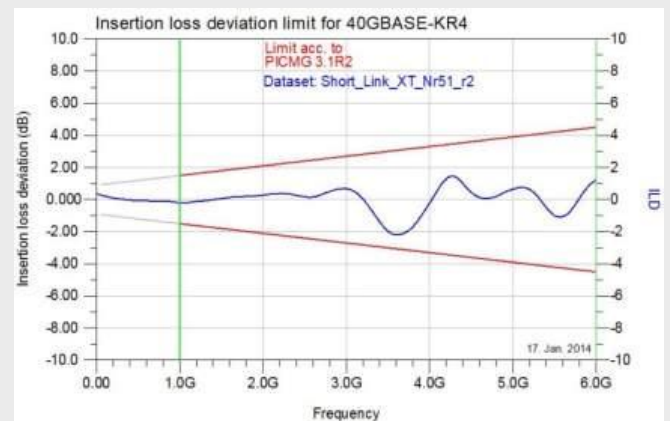


Figure 26: ILD of the shortest worst case channel

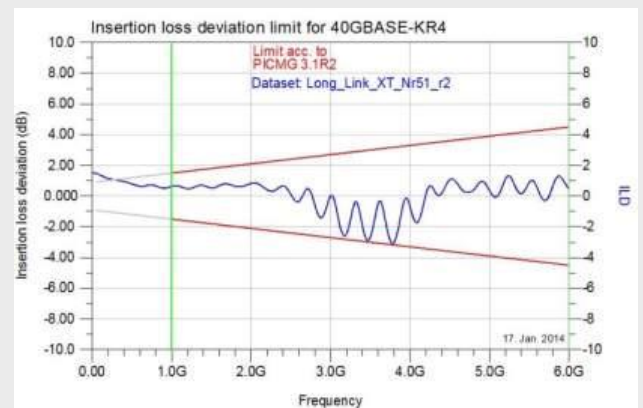


Figure 27: ILD of the longest worst case channel





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## Return loss (RL)

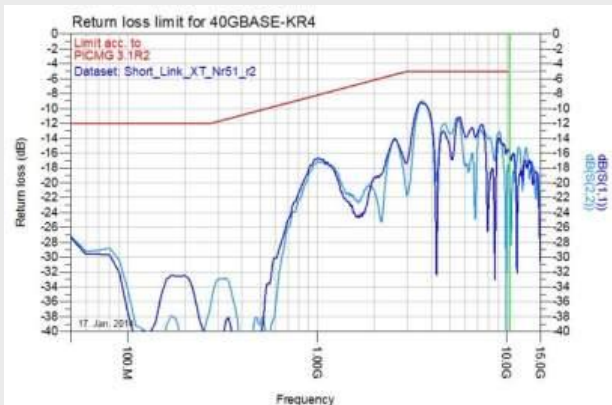


Figure 28: RL of the shortest worst case channel

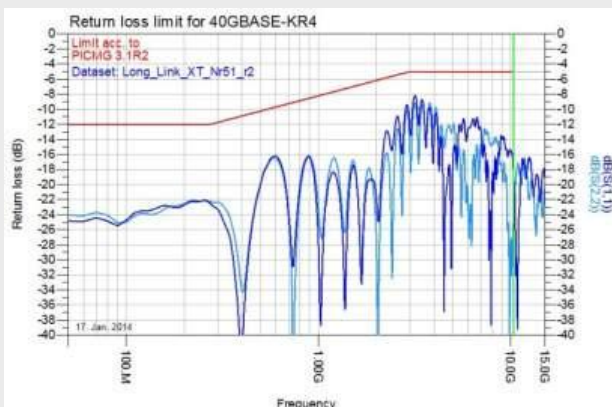


Figure 29: RL of the longest worst case channel

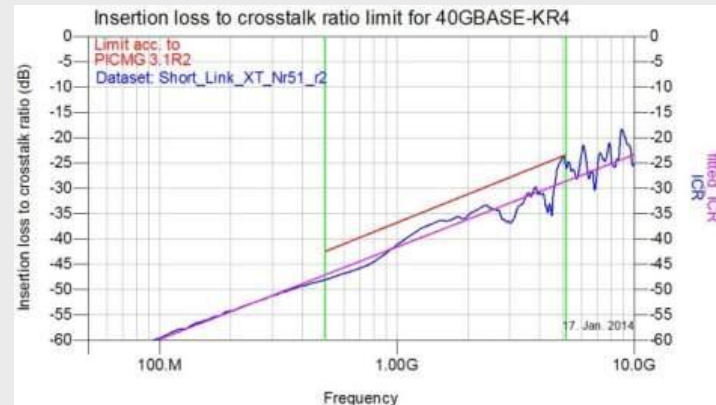


Figure 31: ICR of the shortest worst case channel

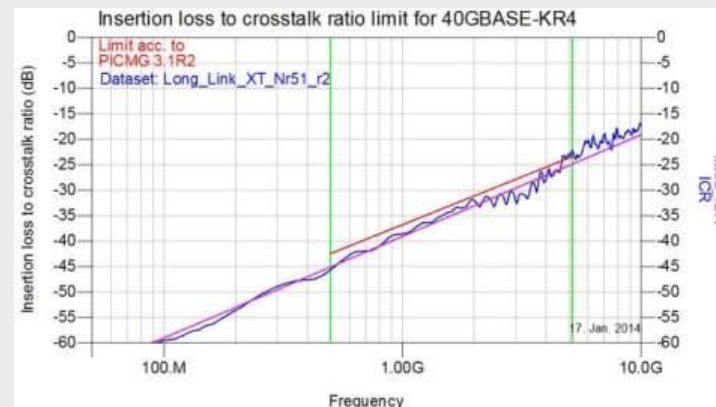


Figure 32: ICR of the longest worst case channel

## Insertion loss to crosstalk ratio (ICR)

One victim pair is surrounded by 6 NEXT (Near-end crosstalk) and 2 FEXT (Far-end crosstalk) aggressors.

	A	B	C	D	E	F	G	H
1	TX2+	TX2-	RX2+	RX2-	TX3+	TX3-	RX3+	RX3-
2	TX0+	TX0-	RX0+	RX0-	TX1+	TX1-	RX1+	RX1-
3	TX2+	TX2-	RX2+	RX2-	TX3+	TX3-	RX3+	RX3-

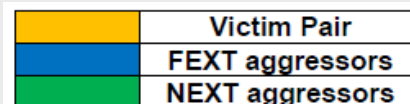


Figure 30: Assignment for crosstalk measurements

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HARTING Integrated Solutions (HIS), as part of HARTING's Connectivity & Networks business unit, designs and manufactures backplanes and backplane systems for all customer-specific applications, including fully integrated systems.

The supply and service range includes backplane PCB design simulation, design validation and signal integrity testing, as well as comprehensive system testing. HIS is active as a fully integrated system developer and manufacturer, including series production. HIS operates a manufacturing „Global footprint“ with factories on three continents: Europe, Asia and North America. Each site has common equipment, tooling and procedures to provide seamless service to all our global customers.

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